Anlogic Technology EG4S20 FPGA Datasheet

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目 录

1 Introduction

1. 1 EAGLE device family features

- Flexible logical structure
  - Equivalent to 23,520 4 input lookup tables
- Low power device
  - Advanced 55nm low power process
  - Static power consumption as low as 5mA
- Rich on-chip storage space
  - Equivalent 23,520 4 input lookup tables (LE)
  - 64Mb SDR SDRAM storage space, up to 200MHz operating frequency
  - Maximum 156.8Kb distributed RAM
  - 64-block 9Kb embedded RAM (EMB9K), 16-block 32Kb embedded RAM
- Configurable logic modules (PLB
  - Optimized LUT4/LUT5 combination design
  - Dual port distributed memory
  - Support for arithmetic logic operations
  - Fast carry chain logic
- Embedded multiplier
  - 29 18 x 18 multipliers supporting 9X9 mode
  - Up to 250MHz
- Source synchronous input/output interface
  - Input/output unit contains DDR register
  - Generic DDRx1
  - Generic DDRx2
- BSCAN
  - Compatible with IEEE-1149.1
- High performance, flexible input/output buffer
  - Support hot swap
  - Configurable pull-up/pull-down mode
  - On-chip 100 ohm differential resistor
  - Configurable Schmitt trigger with a maximum 0.5V hysteresis
- Clock resource
  - 16 global clocks
  - 3 PLLs for frequency synthesis
    - 5 clock outputs
    - Dividing factor 1 to 128
    - Support 5 channels of clock output cascade
    - Dynamic phase selection
- Embedded hard core IP
  - ADC
    - 12-bit successive approximation register type (SAR)
    - Up to 8 analog inputs
    - 1MHz sampling rate (MSPS)
  - Integrated voltage monitoring module
  - Built-in ring oscillator
- Configuration mode
  - Active serial, slave serial, active parallel, slave parallel
  - JTAG mode (IEEE-1532)
  - Support dual boot and multi boot mode
- Package
  - QFN88 BGA256

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Table 1-1 EG4S20 Device Resources

General feature		EG4S20NG88	EG4A20NG88	EG4S20BG256	
Number of FFs		19,600	19,600	19,600	
Number of LUTS		23,520	23,520	23,520	
Number of Dis-Ram bits		156,800	156,800	156,800	
Number of EMB (9k)		64	64	64	
Number of EMB (32k)		16	16	16	
Total EBR bits		1,114,112	1,114,112	1,114,112	
Number of M18x18		29	29	29	
Total Configuration SRAM (bits)		4,988,928	4,988,928	4,988,928	
PLL		3	3	3	
Low-skew gclock in chip		16	16	16	
EM SDR SDRAM		2M X 32bits		2M X 32bits	
User IO Banks		1	1	1	
Maximum user IOs		71	71	193	

Table 1-2 EG4S20 FPGA Package

Packages		EG4S20NG88	EG4A20NG88	EG4S20BG256	
QFN88 (10x10, 0.4mm pitch)		71/14(注)	71/14		
BGA256 (17x17, 1.0mm pitch)				193\92	

Note: Indicates the user available IO number/user available differential output (LVDS) pair

1.2 EG4S20 device features

Anlu's latest EG4S20 FPGA is based on Anlu's proven low-cost, low-power programmable FPGA EG4X20, which is sealed with a 2M X 32bits SDR SDRAM using the latest 3D sealing technology. The EG4S20 FPGA is available in a smaller, simpler and more reliable QFN package, and is available in more IO and more BGA packages. Larger embedded storage capacity, especially suitable for high-capacity, high-speed data acquisition, transmission and conversion applications.

Characteristic advantage

◆ Multi-variety, large capacity built-in storage space

- Built-in 64Mb SDR SDRAM memory space, 32-bit data bus width, up to 200Mhz operating frequency, maximum read/write bandwidth up to 6.4Gbps
- Built-in 64 EMB9K random read/write RAM, configurable as true dual port, simple dual port, single port RAM and FIFO working mode, bit width can be configured as 512x18, 1Kx9, 2Kx4, 4Kx2, 8Kx1, maximum frequency 250Mhz
- Built-in 16 32Kb RAM, configurable as single-port RAM, dual-port RAM, independently configurable as 2Kx16 or 4Kx8

◆ Smaller package, more IO, better for PCB layout

- QFN88 package, EPAD grounded, up to 71 users IO
- BGA256 package, SDRAM built-in, no external user IO, up to 193 users IO
- Supports up to 7 pairs of True LVDS with a maximum frequency of 800Mbps
- QFN88 package, 0.4mm pitch, package size 10mm X 10mm
- BGA256 package, 1.0mm pitch, package size 17mm X 17mm
- Optimized pinouts make it easy to use all of the device's IO with just two layers of PCB
- Supports simple and low-cost SPI FLASH configuration; FLASH can be used as a user after power-on configuration

◆ Integrate multiple dedicated IPs

- Integrated 12BIT SAR ADC with sampling rate up to 1MHz and support for up to 8 input channel multiplexing
- Integrated power monitoring module for specified BANK voltage monitoring
- Integrated internal ring oscillator

2 Hardware design

2.1 EG4S20NG88、EG4A20NG88 pin list

Table 2-1 EG4S20NG88\EG4A20NG88 FPGA Pin List

IO BANK	Name	Pin number	最小系统需要	Second function	Functional description
BANK1	VCC	1	是（注3）		Kernel power
BANK1	IO	2			General IO
BANK1	IO	3			General IO
BANK1	IO	4		LVDS1_N	General IO
BANK1	IO	5		LVDS1_P	General IO
BANK1	GND	6	是		Chip ground
BANK1	VCCIO1	7	是		3.3V BANK1 IO ***Power supply (Note 4)***
BANK1	IO	8	是	DONE	Configuration completed / universal IO
BANK1	VCCIO1	9	是		3.3V BANK1 IO power supply
BANK1	IO	10			General IO
BANK1	IO	11		GCLKIOL_2	General IO
BANK1	IO	12		GCLKIOL_5	General IO
BANK1	IO	13		GCLKIOL_4	General IO
BANK1	IO	14			General IO
BANK2	VCCIO2	15	是		3.3V BANK2 IO power supply
BANK2	IO	16		LVDS2_N	General IO
BANK2	IO	17		LVDS2_P	General IO
BANK2	IO	18			General IO
BANK2	IO	19			General IO
BANK2	VCCIO2	20	是		3.3V BANK2 IO power supply
BANK2	IO	21	是	TDO	JTAG/ General IO
BANK2	IO	22	是	TMS	JTAG/ General IO
BANK3	IO	23			General IO
BANK3	VCCIO3	24	是		BANK3 IO power supply

BANK3	IO	25	是	TDI	JTAG/General IO
BANK3	IO	26	是	TCK	JTAG/ General IO
BANK3	IO	27			General IO
BANK3	IO	28		ELVDS1_N	General IO
BANK3	IO	29		ELVDS1_P	General IO
BANK3	IO	30			General IO
BANK3	IO	31			General IO
BANK3	IO	32		ELVDS2_P	General IO
BANK3	IO	33		ELVDS2_N	General IO
BANK3	IO	34		GCLKIOB_5	General IO
BANK4	IO	35		GCLKIOB_2	General IO
BANK4	VCC	36	是		Kernel power
BANK4	IO	37		ELVDS3_P	General IO
BANK4	IO	38		ELVDS3_N	General IO
BANK4	IO	39			General IO
BANK4	IO	40		ELVDS4_N	General IO
BANK4	IO	41		ELVDS4_P	General IO
BANK4	IO	42			General IO
BANK4	VCCIO4	43	是		BANK4 IO power supply
BANK4	IO	44		HSWAPEN	IO load status / General IO
BANK5	IO	45			General IO
BANK5	VCCIO5	46	是		3.3V BANK5 IO power supply
BANK5	IO	47		LVDS3_P	General IO
BANK5	IO	48		LVDS3_N	General IO
BANK5	IO	49		LVDS4_P	General IO
BANK5	IO	50		LVDS4_N	General IO
BANK5	IO	51			General IO
BANK5	IO	52			General IO
BANK5	VCCIO5	53			3.3V BANK5 IO power supply
BANK5	IO	54		LVDS5_N/GCLKIOR_0	General IO
BANK5	IO	55		LVDS5_P/GCLKIOR_1	General IO

BANK6	VCC	56			Core power
BANK6	IO	57		GCLKIOR_4	General IO
BANK6	VCCIO6	58	是		3.3V BANK6 IO power supply
BANK6	IO	59			General IO
BANK6	IO	60		LVDS6_N	General IO
BANK6	IO	61		LVDS6_P	General IO
BANK6	IO	62			General IO
BANK6	IO	63		LVDS7_N	General IO
BANK6	IO	64		LVDS7_P	General IO
BANK6	VCCIO6	65	是		3.3V BANK6 IO power supply
BANK6	IO	66			General IO
BANK7	IO	67	是	PROGRAM_B	Chip reset/ General IO
BANK7	IO	68	是	INIT_N	General IO
BANK7	IO	69	是	CSO_B	FLASH chip selection General IO
BANK7	IO	70		D3,ELVDS5_P	General IO
BANK7	IO	71		D4,ELVDS5_N	General IO
BANK7	IO	72		D7	General IO
BANK7	VCCIO7	73	是		BANK7 IO power supply
BANK7	IO	74		D6	General IO
BANK7	IO	75		GCLKIOT_7	General IO
BANK7	IO	76		D5	General IO
BANK7	IO	77		GCLKIOT_4/ELVDS6_N	General IO
BANK7	IO	78		GCLKIOT_5/ELVDS6_P	General IO
BANK7	IO	79		GCLKIOB_0	General IO
BANK8	IO	80	是	D0,MISO	FLASH IO/ General IO
BANK8	IO	81	是	MOSI	FLASH IO/ General IO
BANK8	IO	82	是	CCLK	FLASH clock / General IO
BANK8	IO	83	是	M0	Mode selection/ IO

BANK8	IO	84	是	M1, ADC_CH_0	Mode selection / General IO
BANK8	VCCIO8	85	是	ADC_VREF	BANK8 IO power supply
BANK8	IO	86		D1, ADC_CH_5,ELVDS7_P	General IO
BANK8	IO	87		D2, ADC_CH_6,ELVDS7_N	General IO
	VCCAUX	88	是		3.3V auxiliary power supply
	GND	89	是		Chip ground PAD

Note 1: These pins can be used as user IO after the FPGA is powered up by software configuration.

Note 2: Refer to the EG4 FPGA manual. DPCLK, GCLKIO, and GPLL_CLKIN can be used as PLL dedicated clock inputs with fixed input delay.

Note 3: These pins are the minimum system requirements of the chip. It must be ensured that these pins are properly connected for the chip to work properly.

Note 4: BANK1, BANK2, BANK3, BANK4, BANK5, BANK6, BANK7 of EG4S20NG88 devices must use 3.3V IO voltage, BANK8 can support 1.2V, 1.5V, 1.8V, 2.5V, 3.3V IO level.

BANK3, BANK4, and BANK7 of the EG4A20NG88 device must use 3.3V IO voltage, and other BANKs support 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V IO levels.

2.2 EG4S20BG256 pin list

Table 2-2 EG4S20BG256 FPGA Pin List

编号	BANK	引脚说明		编号	BANK	引脚说明
P16	1	IO_L1P_1		G12	1	IO_L13P_1
P15	1	IO_L1N_1		L16	1	IO_L14P_1
L12	1	IO_L2P_1		M16	1	IO_L14N_1
M11	1	IO_L2N_1		J16	1	IO_L15P_1
P13	1	IO_L3P_1,DONE		K16	1	IO_L15N_1
P14	1	IO_L3N_1		D16	1	IO_L16N_1
K11	1	IO_L4P_1		D14	1	IO_L16P_1
J11	1	IO_L4N_1		F15	1	IO_L17P_1
L13	1	IO_L5P_1		E15	1	IO_L17N_1
M13	1	IO_L5N_1		G16	1	IO_L18P_1
L14	1	IO_L6P_1		H16	1	IO_L18N_1
M14	1	IO_L6N_1		E14	1	IO_L_1,TDO
M15	1	IO_L7N_1		A15	1	IO_L_1,TMS
K15	1	IO_L7P_1				
K12	1	IO_L8P_GCLKIOL_3_1				
J12	1	IO_L8N_GCLKIOL_2_1				
K14	1	IO_L_GCLKIOL_4_1				
J14	1	IO_L_1				
H14	1	IO_L_1				
J13	1	IO_L9N_1				
H13	1	IO_L9P_1				
N14	1	IO_L10P_1				
N16	1	IO_L10N_1				
H15	1	IO_L11P_1				
G14	1	IO_L11N_1				
F14	1	IO_L12N_1				
F13	1	IO_L12P_1				
G11	1	IO_L13N_1				

编号	BANK	引脚说明		编号	BANK	引脚说明
F16	0	IO_BE1N_0		C16	0	IO_BE13P_0
E16	0	IO_BE1P_0		B14	0	IO_BE14P_0
C12	0	IO_B_0,TDI		A14	0	IO_BE14N_0
C14	0	IO_B_0,TCK		B15	0	IO_BE15N_0
E12	0	IO_BE2N_0		B16	0	IO_BE15P_0
F12	0	IO_BE2P_0		C8	0	IO_BE16P_0
F10	0	IO_BE3P_0		B8	0	IO_BE16N_0
H11	0	IO_BE3N_0		A12	0	IO_BE17N_0
D12	0	IO_BE4N_0		A13	0	IO_BE17P_0
D11	0	IO_BE4P_0		A8	0	IO_BE18P_0
E10	0	IO_BE5N_0		A7	0	IO_BE18N_0
E11	0	IO_BE5P_0		C7	0	IO_BE19N_0
E13	0	IO_BE6P_0		C6	0	IO_BE19P_0
C13	0	IO_BE6N_0		A5	0	IO_BE20P_0
C10	0	IO_BE7N_0		A6	0	IO_BE20N_0
B12	0	IO_BE7P_0		B6	0	IO_BE21N_0
C11	0	IO_BE8P_0		C5	0	IO_BE21P_0
A11	0	IO_BE8N_0		E7	0	IO_BE22N_0
F9	0	IO_BE9P_GCLKIOB_1_0		F7	0	IO_BE22P_0
D9	0	IO_BE9N_GCLKIOB_0_0		E6	0	IO_BE23P_0
C9	0	IO_BE10N_GCLKIOB_4_0		F6	0	IO_BE23N_0
B10	0	IO_BE10P_GCLKIOB_5_0		A4	0	IO_BE24N_0
A10	0	IO_BE11P_GCLKIOB_7_0		A3	0	IO_BE24P_0
A9	0	IO_BE11N_GCLKIOB_6_0		D5	0	IO_BE25P_0
E8	0	IO_BE12N_GCLKIOB_2_0		D6	0	IO_BE25N_0
D8	0	IO_BE12P_GCLKIOB_3_0		B5	0	IO_BE26N_0
C15	0	IO_BE13N_0		C4	0	IO_BE26P_0,HSWAPEN

编号	BANK	引脚说明		编号	BANK	引脚说明
D3	3	IO_R1N_3		H2	3	IO_R13P_GCLKIOR_7_3
B3	3	IO_R1P_3		L1	3	IO_R13N_GCLKIOR_6_3
E4	3	IO_R2N_3		H3	3	IO_R14N_GCLKIOR_0_3
E3	3	IO_R2P_3		H4	3	IO_R14P_GCLKIOR_1_3
F4	3	IO_R3N_3		J4	3	IO_R15N_GCLKIOR_4_3
F5	3	IO_R3P_3		J3	3	IO_R15P_GCLKIOR_5_3
B2	3	IO_R4P_3		K2	3	IO_R16N_3
A2	3	IO_R4N_3		K3	3	IO_R16P_3
B1	3	IO_R_3		J6	3	IO_R17N_3
C3	3	IO_R5P_3		K5	3	IO_R17P_3
C2	3	IO_R5N_3		P1	3	IO_R18P_3
F3	3	IO_R_3		R1	3	IO_R18N_3
C1	3	IO_R6P_3		P2	3	IO_R19N_3
E2	3	IO_R6N_3		R2	3	IO_R19P_3
D1	3	IO_R7N_3		M2	3	IO_R20N_3
E1	3	IO_R7P_3		L3	3	IO_R20P_3
F2	3	IO_R8N_3		K6	3	IO_R21P_3
F1	3	IO_R8P_3		M3	3	IO_R21N_3
G6	3	IO_R9N_3		L4	3	IO_R_3
G5	3	IO_R9P_3		L5	3	IO_R_3
G3	3	IO_R10N_3		N3	3	IO_R22N_3
G1	3	IO_R10P_3		M4	3	IO_R22P_3
H5	3	IO_R11N_3		P4	3	IO_R23P_3
H1	3	IO_R11P_3		N4	3	IO_R23N_3
J1	3	IO_R12N_3		M5	3	IO_R_3
K1	3	IO_R12P_3		M1	3	IO_R24N_3
				N1	3	IO_R24P_3

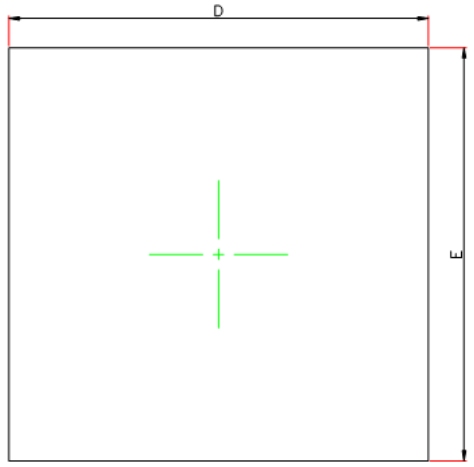
引脚	BANK	引脚说明		编号	BANK	引脚说明
T2	2	IO_T_2,PROGRAM_B		T13	2	IO_TE13N_GCLKIOT_2_2
R3	2	IO_T_2,INIT_B		T14	2	IO_TE13P_GCLKIOT_3_2
T3	2	IO_T_2,CSO_B		P10	2	IO_T_2,D0_DIN_MISO
T4	2	IO_TE1N_2		T10	2	IO_T_2,MOSI_CSI_B
P6	2	IO_TE1P_2		T15	2	IO_TE15N_2
T5	2	IO_TE2P_2		R15	2	IO_TE15P_2
T6	2	IO_TE2N_2		R14	2	IO_TE16P_2
N5	2	IO_TE3P_2,D3		R12	2	IO_TE16N_2
P5	2	IO_TE3N_2,D4		T11	2	IO_T_2,M0
M6	2	IO_TE4P_2		R11	2	IO_T_2,CCLK
N6	2	IO_TE4N_2		M10	2	IO_TE17P_2,ADC_CH_1
M7	2	IO_TE5N_2		P11	2	IO_TE17N_2,ADC_CH_3
T12	2	IO_TE5P_2		L10	2	IO_T_2,ADC_CH_2
R5	2	IO_TE6P_2,D7		N11	2	IO_T_2,M1,ADC_CH_0
P8	2	IO_TE6N_2		N12	2	IO_TE18P_2,D1,ADC_CH_5
N8	2	IO_TE7N_2		P12	2	IO_TE18N_2,D2,ADC_CH_6
T9	2	IO_TE7P_2		R16	2	IO_TE19N_2,ADC_CH_7
R9	2	IO_TE8P_2		M12	2	IO_TE19P_2,ADC_CH_4
P9	2	IO_TE8N_2				
L7	2	IO_TE9N_2,D6				
L8	2	IO_TE9P_2,D5				
P7	2	IO_TE10P_GCLKIOT_7_2				
M9	2	IO_TE10N_GCLKIOT_6_2				
T7	2	IO_TE11N_GCLKIOT_4_2				
R7	2	IO_TE11P_GCLKIOT_5_2				
N9	2	IO_TE12P_GCLKIOT_1_2				
T8	2	IO_TE12N_GCLKIOT_0_2				

编号	BANK	引脚说明		编号	BANK	引脚说明
L11	-	ADC_VREF		G7	-	VCCINT
B13	-	VCCO_0		G9	-	VCCINT
B4	-	VCCO_0		H10	-	VCCINT
B9	-	VCCO_0		H8	-	VCCINT
D10	-	VCCO_0		J7	-	VCCINT
D7	-	VCCO_0		J9	-	VCCINT
D15	-	VCCO_1		K10	-	VCCINT
G13	-	VCCO_1		K8	-	VCCINT
J15	-	VCCO_1		A1		GND
K13	-	VCCO_1		A16		GND
N15	-	VCCO_1		B11		GND
R13	-	ADC_VDDA		B7		GND
N10	-	VCCO_2		D13		GND
N7	-	VCCO_2		D4		GND
R4	-	VCCO_2		E9		GND
R8	-	VCCO_2		G15		GND
D2	-	VCCO_3		G2		GND
G4	-	VCCO_3		G8		GND
J2	-	VCCO_3		H12		GND
K4	-	VCCO_3		H7		GND
N2	-	VCCO_3		H9		GND
E5	-	VCCAUX		J5		GND
F11	-	VCCAUX		J8		GND
F8	-	VCCAUX		K7		GND
G10	-	VCCAUX		K9		GND
H6	-	VCCAUX		L15		GND
J10	-	VCCAUX		L2		GND

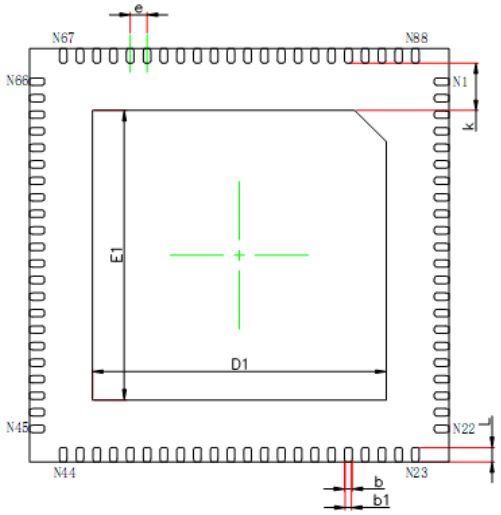
L6	-	VCCAUX		M8		GND
L9	-	VCCAUX		N13	-	GND
P3	-	GND		T1		GND
R10		GND		T16		GND
R6		GND				

Note: Because BANK1 and BANK3 internal IO are connected to SDR SDRAM, VCCO1 and VCCO3 can only be connected to 3.3V power supply.

2.3 EG4S20NG88 package size



TOP VIEW

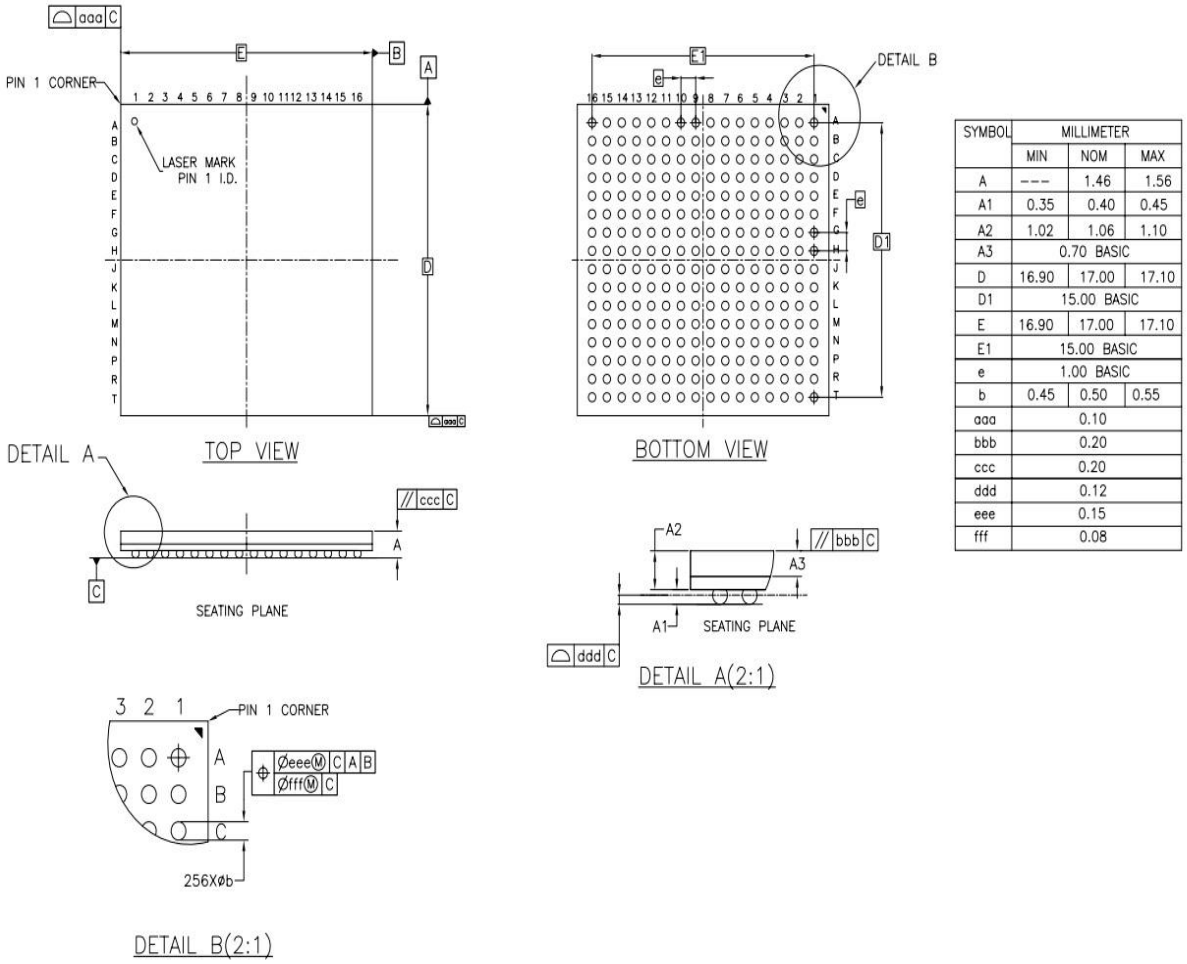


SIDE VIEW

BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	9.924	10.076	0.391	0.397
E	9.924	10.076	0.391	0.397
D1	6.900	7.100	0.272	0.280
E1	6.900	7.100	0.272	0.280
k	1.150REF.		0.045REF.	
b	0.150	0.250	0.006	0.010
b1	0.100	0.200	0.004	0.008
e	0.400BSC.		0.016BSC.	
L	0.274	0.426	0.011	0.017

2.4 EG4S20BG256 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	1.46	1.56
A1	0.35	0.40	0.45
A2	1.02	1.06	1.10
A3	0.70 BASIC		
D	16.90	17.00	17.10
D1	15.00 BASIC		
E	16.90	17.00	17.10
E1	15.00 BASIC		
e	1.00 BASIC		
b	0.45	0.50	0.55
aaa	0.10		
bbb	0.20		
ccc	0.20		
ddd	0.12		
eee	0.15		
fff	0.08		

2.5 EG4S20NG88 minimum hardware system

For the EG4S20NG88 FPGA to work properly, it is necessary to ensure that the minimum system shown in Table 2-1 requires the relevant pins to be properly connected. For hardware design examples, please refer to the appendix EG4S20NG88_FPGA_CORE.pdf.

2.6 EG4A20NG88 device

The EG4A20NG88 chip does not contain SDR SDRAM internally, and other internal resources and external pins are identical to the EG4S20NG88 device.

The BANK3, BANK4, and BANK7 of the EG4A20NG88 device only support 3.3V IO voltage. Other BANKs support 1.2V, 1.8V, 2.5V, 3.3V IO voltage.

3 Use internal SDR SDRAM

The EG4S20 embeds a 2M X 32bit SDRAM with a maximum operating frequency of 200Mhz and a maximum read/write bandwidth of 6.4Gbps. SDRAM and FPGA are deeply integrated by software, so if you want to use SDRAM, you only need to implement the following IP module at the top level. The prototype of this IP is as follows:

```
EG_PHY_SDRAM_2M_32  U_EG_PHY_SDRAM_2M_32(

                .clk(SD_CLK),                   // SDRAM clock 1 bit width

                .ras_n(SD_RAS_N),               // SDRAM row strobe 1 bit width

                .cas_n(SD_CAN_N),               //SDRAM column strobe 1 bit width
                .we_n(SD_WE_N),                 //SDRAM write enable 1bit bit width
                .addr(SD_SA),                   //SDRAM address 11bits bit width
                .ba(SD_BA),                     // SDRAM BANK address 2bits bit width
                .dq(SD_DQ),                     //  SDRAM data 32bits bit width
                .cke(SD_CKE),                   //  SDRAM clock enable 1bit bit width
                .dm(4'd0)                       //   SDRAM data mask 4bits bit width
);
```

Table 3-1 SDRAM Pin Assignment

SDRAM pin name	SDRAM pin description	Pin connection
DQ0	Data pin 0	与 IP 相连 (Connected to IP)
DQ1	Data pin 1	与 IP 相连
DQ2	Data pin 2	与 IP 相连
DQ3	Data pin 3	与 IP 相连
DQ4	Data pin 4	与 IP 相连
DQ5	Data pin 5	与 IP 相连
DQ6	Data pin 6	与 IP 相连
DQ7	Data pin 7	与 IP 相连
DQ8	Data pin 8	与 IP 相连
DQ9	Data pin 9	与 IP 相连
DQ10	Data pin 10	与 IP 相连
DQ11	Data pin 11	与 IP 相连
DQ12	Data pin 12	与 IP 相连
DQ13	Data pin 13	与 IP 相连
DQ14	Data pin 14	与 IP 相连
DQ15	Data pin 15	与 IP 相连
DQ16	Data pin 16	与 IP 相连
DQ17	Data pin 17	与 IP 相连
DQ18	Data pin 18	与 IP 相连
DQ19	Data pin 19	与 IP 相连
DQ20	Data pin 20	与 IP 相连
DQ21	Data pin 21	与 IP 相连
DQ22	Data pin 22	与 IP 相连
DQ23	Data pin 23	与 IP 相连
DQ24	Data pin 24	与 IP 相连
DQ25	Data pin 25	与 IP 相连
DQ26	Data pin 26	与 IP 相连
DQ27	Data pin 27	与 IP 相连
DQ28	Data pin 28	与 IP 相连

DQ29	Data pin 29	与 IP 相连
DQ30	Data pin 30	与 IP 相连
DQ31	Data pin 31	与 IP 相连
SA0	Address pin 0	与 IP 相连
SA1	Address pin 1	与 IP 相连
SA2	Address pin 2	与 IP 相连
SA3	Address pin 3	与 IP 相连
SA4	Address pin 4	与 IP 相连
SA5	Address pin 5	与 IP 相连
SA6	Address pin 6	与 IP 相连
SA7	Address pin 7	与 IP 相连
SA8	Address pin 8	与 IP 相连
SA9	Address pin 9	与 IP 相连
SA10	Address pin 10	与 IP 相连
BA0	BANK address pin 0	与 IP 相连
BA1	BANK address pin 1	与 IP 相连
WE_N	Write enable	与 IP 相连
RAS_N	Line strobe	与 IP 相连
CAS_N	Column strobe	与 IP 相连
CLK	Chip clock	与 IP 相连
CS_N	Chip Select	与 IP 相连
DM0	Data 0-7 Shielding	与 IP 相连
DM1	Data 8-15 Shielding	与 IP 相连
DM2	Data 16-23 Shielding	与 IP 相连
DM3	Data 24-31 Shielding	与 IP 相连
CKE	Clock enable	与 IP 相连

4 Software usage wizard

4. 1 Special IP use

1. IO delay unit, which can be used to adjust the input delay of the RGMII signal.

```
EG_LOGIC_IDELAY    U0_EG_LOGIC_IDELAY(
                        .i(PHY1_RXDV),
                        .o(rxdv_int));
defparam U0_EG_LOGIC_IDELAY.INDEL = 0;
```

After this unit, the initial increase of 0.8ns delay, the parameter is used to set the delay length, each increase 1, increase the delay 0.1ns; parameter adjustment range is 0-31.

2. Input dual edge sampling unit for double edge sampling of RGMII input signal

```
EG_LOGIC_IDDR    IDDR_0(
                        .q0(rxd_r2g_tmp[3]),
                        .q1(rxd_r2g_tmp[7]),
                        .clk(rxc),
                        .d(rxd[3]),
                        .rst(~rst_n));
```

3. The output dual edge drive unit for dual edge drive of the RGMII output signal

```
EG_LOGIC_ODDR    ODDR_0(
                        .q(txd[0]),
                        .clk(txc_tmp),
                        .d0(txd_tmp[4]),
                        .d1(txd_tmp[0]),
                        .rst(RST_OUT0));
```

4. An internal restart control unit for the program control chip to restart from the specified address of the FLASH loader

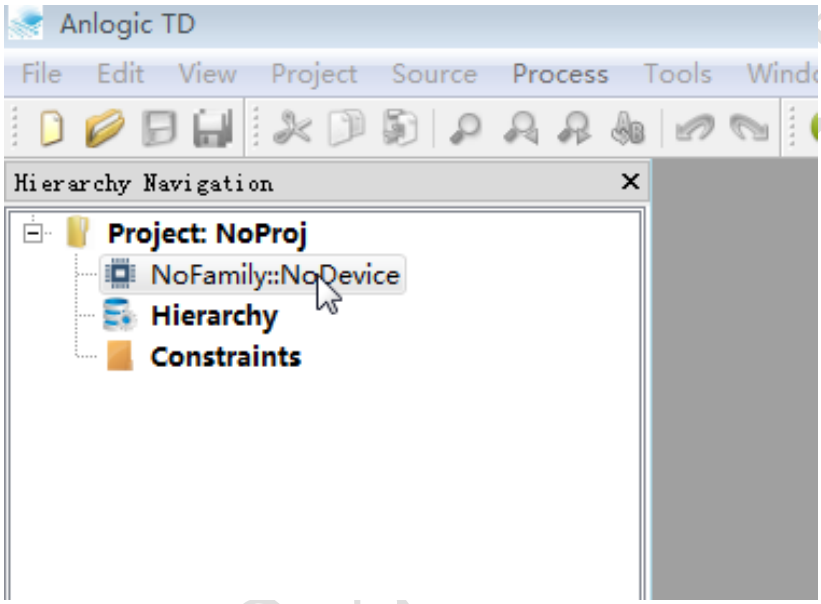
```
EG_LOGIC_MBOOT    U_EG_LOGIC_MBOOT(
                        .rebootn(rebootn),
                        .dynamic_addr(dynamic_addr));
```

The dynamic start-up address is set in dynamic_addr, which is the upper 8 bits of the 24-bit FLASH address, and then a low pulse is input on rebootn to trigger the FPGA reload.

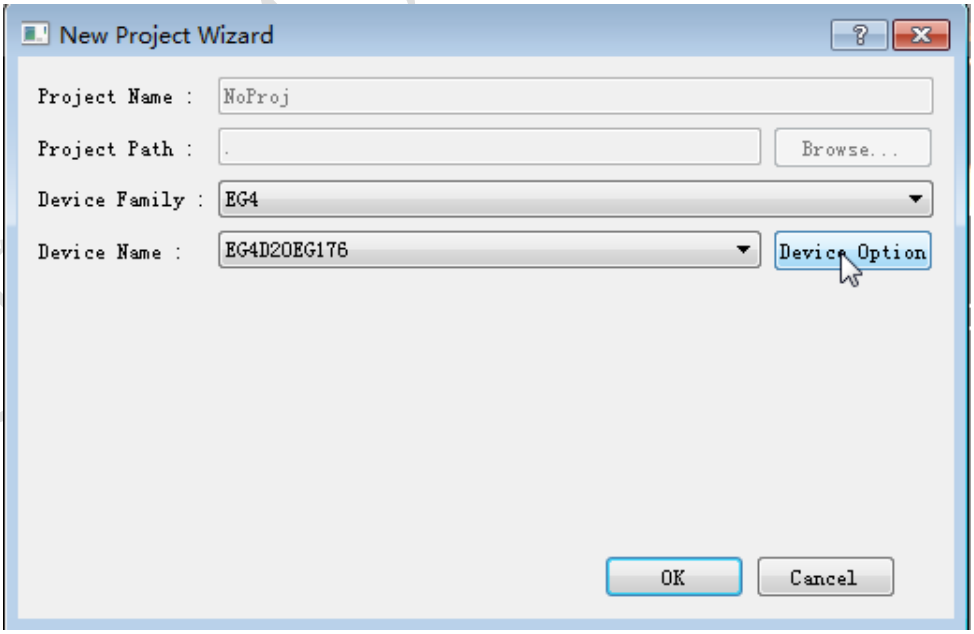
5. Dual function pin settings

1) Signals such as PROGRAM_B, CSO_B, DO_DIN_MISO, MOSI_CSI_B, CCLK, DONE, JTAG_TMS, JTAG_TCK, JTAG_TDO, JTAG_TDI can be set to general-purpose IO or dedicated pins by software. The setup steps are as follows:

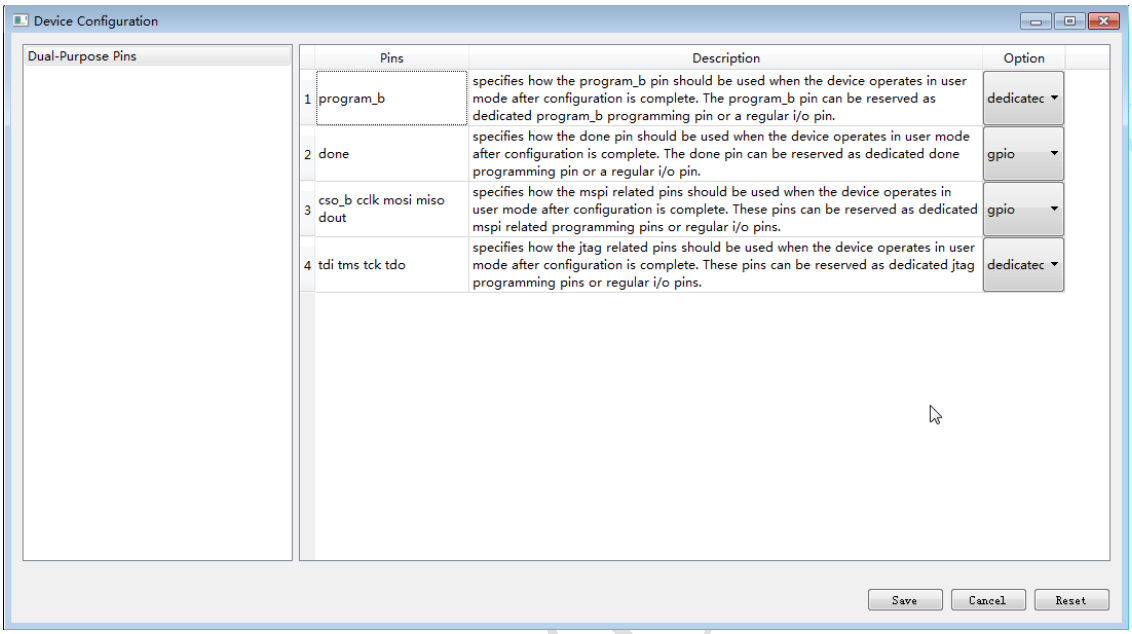
a. Double-click the device in the project bar and jump out of the device selection interface in the second step.



b. Click the DeviceOption box

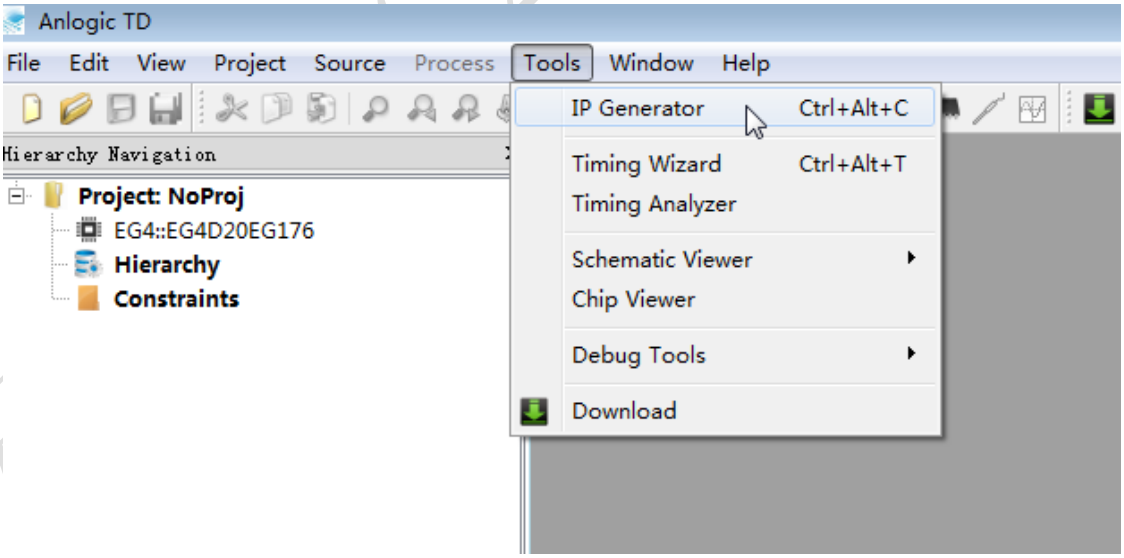


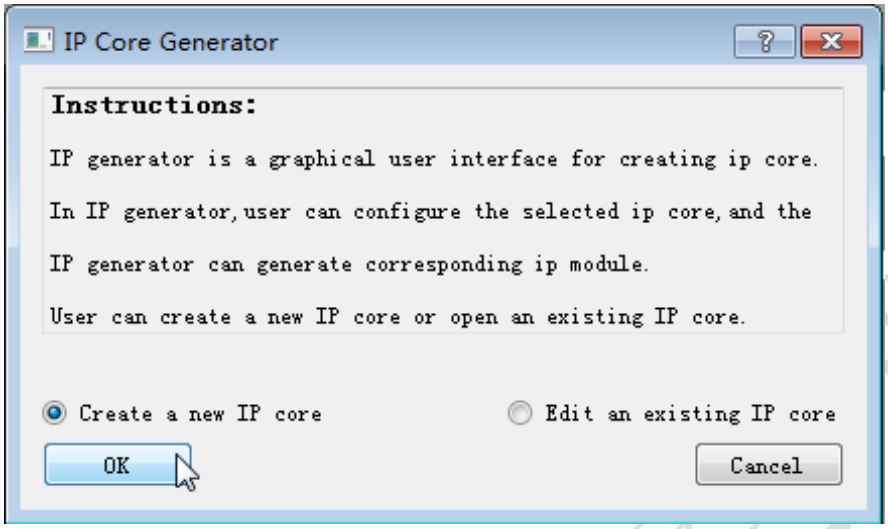
c. After jumping out of the dual function pin setting interface of the figure below, you can set whether the pin is dedicated function pin or used as GPIO at the corresponding pin to be set. Special attention is required. If the JTAG pin is used as a GPIO, the JTAG interface cannot be used to control the FPGA after the FPGA has successfully loaded the program.



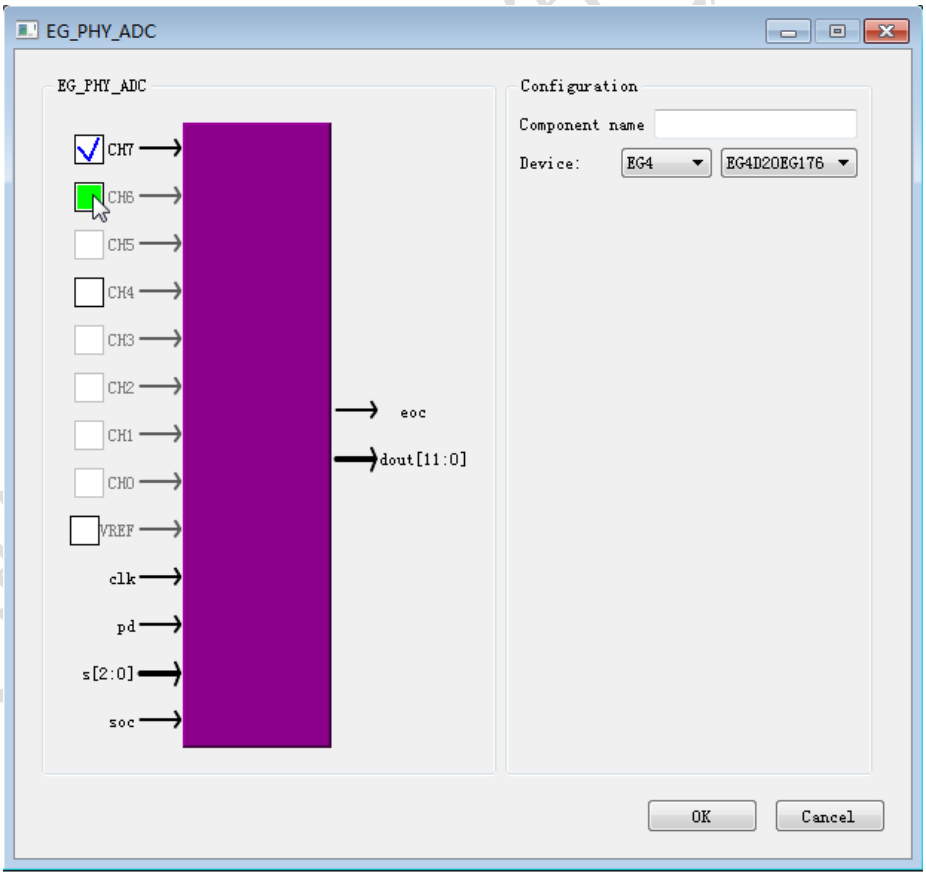
2)ADC Input ADC_CHx Signal Multiplex Pin Settings

a. Click on "Tools" and select "Ip Generator" to create or open an ADC IP.





b. Enter the ADC IP setting interface, tick the front of the channel that needs to be opened, the software will automatically set the pin to the dedicated function pin or use it as GPIO.



Note: Please refer to Eagle_DataSheet_v2.0.pdf for specific device resources and usage details.

5 Version Information

Date	Version	Revision
08/04/2017	1.0	First release of Chinese version
12/11/2017	1.1	Add EG4S20BG256 device
5/23/2018	1.5	Correct EG4S20BG256 device N14 N16 differential pair error